removing a portion of said top electrode layer to expose a portion of the dielectric layer, thereby forming a top electrode;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer, wherein a portion of the dielectric is removed from an intermediate region between the top electrode and the bottom electrode layer;

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer, whereby a portion of the conformal insulating layer is formed in said intermediate region; and

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the conformal insulating layer.--

Please replace claim 4 with the following (a marked up version is in the Appendix):

--4.(Thrice Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer, thereby forming a top electrode;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer, wherein a portion of the dielectric is removed from an intermediate region between the top electrode and the bottom electrode layer;

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer, whereby a portion of the conformal insulating layer is formed in said intermediate region; and

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forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of conformal insulating layer, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.--

Please replace claim 15 with the following (a marked up version is in the Appendix):

--15.(Twice Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer, thereby forming a top electrode;

forming an insulating layer over at least a portion of said top electrode and said exposed portion of the dielectric layer;

removing a portion of said insulating layer and a portion of said dielectric layer, thereby exposing at least a portion of said lower electrode layer and forming side wall spacers, wherein said side wall spacers are formed on the side walls of the top electrode and of the inter-electrode region of the dielectric and wherein the top of the top electrode is exposed; and

forming a non-insulating layer over at least a portion of the [structure subsequent removing a portion of said insulating layer and a portion of said dielectric layer] top electrode, the side wall spacers and the lower electrode layer, wherein said non-insulating layer is an anti-reflective layer (ARL) for use in a photolithographic process.--

Please replace claim 26 with the following (a marked up version is in the Appendix):

--26.(Twice Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

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removing a portion of said top electrode layer to expose a portion of the dielectric layer thereby forming a top electrode, wherein the bottom electrode layer is not exposed;

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of said top electrode and said exposed portion of the dielectric layer; and

subsequently removing a portion of said exposed portion of the dielectric layer and a portion of said bottom electrode layer, thereby exposing at least a portion of said semiconductor body and forming one or more capacitors.--

Please replace claim 36 with the following (a marked up version is in the Appendix):

--36.(Twice Amended) A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

forming a capacitor structure, comprising:

a top electrode over a portion of said conductive layer; and

a dielectric layer between said top electrode and said conductive layer;

forming a conformal insulating layer over said capacitor structure and at least a portion of said conductive layer proximate to capacitor structure, whereby a portion of said conformal layer is formed in the region between the top electrode and the conductive layer;

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the [structure resultant from said forming a] conformal layer;

forming a patterned mask over the ARL; and

etching said conductive layer using said patterned mask.--

Please add the following new claims:

--72.(New) The method of claim 3, further comprising:

forming a photoresist over at least a portion of the anti-reflective layer; and

irradiating said photoresist, wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates said photoresist by 70% or more.

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73.(New) The method of claim 72, wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates said photoresist by 70% to 85%.

74.(New) The method of claim 3, wherein said anti-reflective layer is a Si_xON_y film.

75.(New) The method of claim 15, further comprising:

forming a photoresist over at least a portion of the anti-reflective layer; and

irradiating said photoresist, wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates said photoresist by 70% or more.

76.(New) The method of claim 75, wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates said photoresist by 70% to 85%.

77.(New) The method of claim 15, wherein said anti-reflective layer is a Si_xON_y film.

78.(New) The method of claim 26, further comprising:

forming a photoresist over at least a portion of said anti-reflective layer;

irradiating said photoresist, wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates said photoresist by 70% or more; and

subsequently etching a portion of said exposed portion of the dielectric layer and a portion of said bottom electrode layer using said photoresist, thereby exposing at least a portion of said semiconductor body and forming one or more capacitors.

79.(New) The method according to claim 78, wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates said photoresist by 70% to 85%.

80.(New) The method according to claim 26, wherein said anti-reflective layer is a Si_xON_y film.

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81.(New) A method of forming an integrated circuit, comprising:

a process flow for forming one or more transistors including:

forming a conductive layer on a semiconductor body;

subsequently forming an anti-reflective layer; and

defining and etching the conductive layer using the anti-reflective layer; and

an optional capacitor process module including, subsequent to said forming a conductive layer and prior to said forming an anti-reflective layer:

forming a top capacitor electrode over a portion of said conductive layer; and

forming a dielectric layer between said top electrode and said conductive layer, wherein said defining and etching the conductive layer forms the gate of one or more transistors and a bottom capacitor electrode,

wherein the process parameters of said process flow for forming one or more transistors are optimized for the case when the optional capacitor process module is omitted, and wherein the process parameters for the optional capacitor module are optimized for capacitor formation while maintaining the process parameters of said process flow for forming one or more transistors optimized for the case when the capacitor process module is omitted.

82.(New) The method of claim 81, wherein said optional capacitor process module comprises:

forming a dielectric layer over at least a portion said conductive layer;

forming a top electrode layer over at least a portion of said conductive layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer, thereby forming said top capacitor electrode;

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removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said conductive layer, thereby forming said dielectric layer between said top electrode and said conductive layer; and

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the conductive layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer.

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83.(New) The method of claim 82, wherein the thickness of said conformal insulating layer is selected to optimize the capacitor formation while maintaining the process parameters of said process flow for forming one or more transistors optimized for the case when the capacitor process module is omitted.

84.(New) The method of claim 82, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

85.(New) The method of claim 81, wherein said defining and etching the conductive layer using the anti-reflective layer comprises:

forming the anti-reflective layer over the conductive layer and, when the optional capacitor process module is included, the top capacitor electrode and the dielectric layer between said top electrode and said conductive layer;

forming a patterned mask over the anti-reflective layer; and

and etching said conductive layer using said patterned mask.--

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